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Short Note

Difference between Traps Determined from Transient Capacitance and Transient Reverse Current

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The densities and energy levels of traps in silicon pin diodes are determined using the transient capacitance method (ICTS: isothermal capacitance transient spectroscopy) as well as the transient reverse current method (DCTS: discharge current transient spectroscopy). The traps determined by ICTS are located in the i layer (i.e., the n^- region) and affect the steady-state reverse current (i.e., a generation current). Conversely, the traps determined by DCTS are probably located at the surface of the substrate.

KEYWORDS: transient reverse current, steady-state reverse current, pin diode, determination of trap densities and trap levels, discharge current transient spectroscopy, isothermal capacitance transient spectroscopy, surface states, generation centers

One of the authors has developed a method for graphically determining the densities (N_t) and energy levels (E_t) of traps related to the transient current, called discharge current transient spectroscopy (DCTS).[1–3] Although DCTS was proposed for the determination of such in insulators, it can determine N_t and E_t of traps (T_{DCTS}) related to the transient reverse current in diodes. Another method, isothermal capacitance transient spectroscopy (ICTS),[4] can determine N_t and E_t of traps (T_{ICTS}) related to the transient capacitance in diodes. Using silicon (Si) pin diodes for X-ray detectors, we investigate the difference between traps determined by DCTS and those determined by ICTS. Moreover, we study the relationship between these traps and the steady-state reverse current.

The resistivity and thickness of phosphorus (P)-doped n-type Si substrate (i.e., an i layer) were approximately 2 kΩ·cm and 300 μm, respectively. A 0.2-μm-thick n^+ layer was formed on one side of the substrate by the thermal diffusion of P, and then 0.15-μm-thick p^+ layers with a circle 3 mm in diameter were formed on the other side by the thermal diffusion of boron (B). The junction area (S) of the pin diode was 7.1 mm^2. Except the p^+ regions, the surface of this side was passivated with silicon dioxide (SiO_2). Chips with an area of 5 mm × 5 mm were fabricated by dicing the substrate. The diced edge was not passivated.

The current–voltage (I–V) characteristics and the transient reverse currents were measured using a Keithley 236 Source Measure Unit. The capacitance–voltage (C–V) characteristics and the transient capacitance were measured at 1 MHz using a Horiba DA-1500.

From the slope of the $1/C^2$–V curve, the density (N_{sum}) was determined to be 2.4×10^{12} cm^{-3}. N_{sum} indicates the sum of the donor density (N_D) and the density of positively charged traps in the depletion region.

The ICTS signal is defined by[4]

$$S(t) \equiv t\frac{\mathrm{d}C(t)^2}{\mathrm{d}t}, \tag{1}$$

where $C(t)$ is the transient capacitance after a reverse bias voltage (V_R) is applied to the pin diode ($t = 0$ s). Since

$$S(t_{peak}) = N_t\frac{C_\infty^2 \exp(-1)}{N_{sum}} \tag{2}$$

at the peak time ($t_{peak} = 1/e_t$), the values of N_t and e_t can be determined from $S(t_{peak})$ and t_{peak}, respectively, where C_∞ is the steady-state capacitance at V_R and e_t is the emission rate for electrons.

Figure 1 shows the ICTS signal at $V_R = -30$ V at room temperature. The values of t_{peak} and N_t were obtained to be 1.0×10^{-3} s and 1.2×10^{12} cm^{-3}, respectively. From the filling pulse measurement,[4] the capture cross section (σ_t) of T_{ICTS} was determined to be 1.4×10^{-15} cm^2. Using σ_t,[4] E_t was determined to be $E_C - 0.53$ eV, where E_C is the energy level at the bottom of the conduction band. Judging from the magnitude of σ_t, T_{ICTS} is neutral in the depletion region and is negative in the bulk. Therefore, N_D is 2.4×10^{12} cm^{-3}, and the electron concentration (n) in the conduction band is 1.2×10^{12} cm^{-3} in the bulk.

The DCTS signal is defined by[1–3]

$$D(t) \equiv t\,[I_{dis}(t) - I_\infty]\,\frac{\exp(1)}{q}, \tag{3}$$

where $I_{dis}(t)$ is the transient reverse current after V_R is applied to the pin diode ($t = 0$ s), I_∞ is the steady-state reverse current at V_R and q is the magnitude of an electron charge. The peak value of $D(t)$ is expressed as[3]

$$D(t_{peak}) = A_t, \tag{4}$$

where $t_{peak} = 1/e_t$ and A_t is the number of captured carriers at $t = 0$ s.

Figure 2 shows the temperature dependence of DCTS signals at $V_R = -100$ V. Each measurement was carried out after the diode was kept at 0 V for one day. From the peak value, A_t of T_{DCTS} was determined to be about 6.8×10^{15} electrons. If T_{DCTS} is uniformly located in the i layer, N_t is

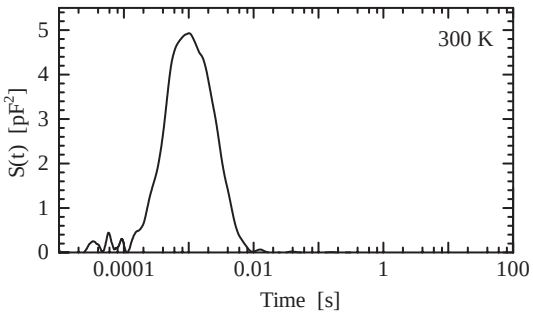

Fig. 1. ICTS signal at 10^{-5} s $< t < 10^2$ s for a reverse bias of -30 V. After the bias was kept at 0 V for 1 ms, ICTS measurements were performed.

*Web site: http://www.osakac.ac.jp/labs/matsuura/

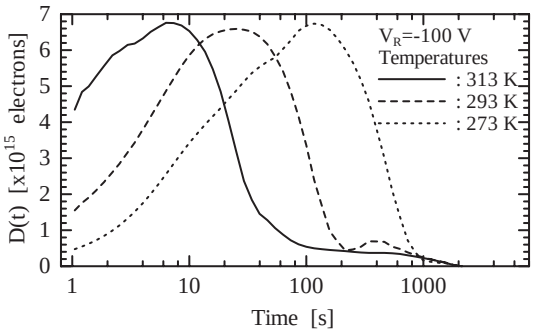

Fig. 2. Temperature dependence of DCTS signals for a reverse bias of −100 V. Each DCTS measurement was carried out after the diode was kept at 0 V for one day.

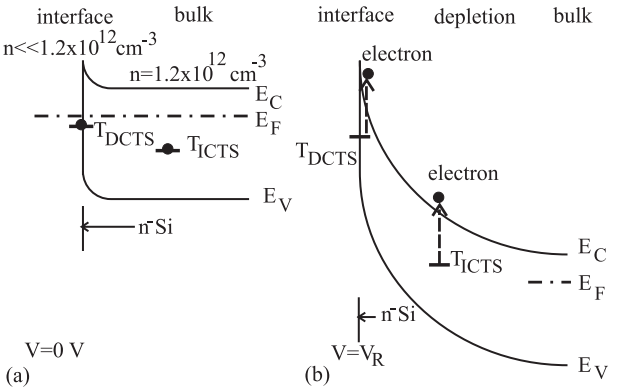

Fig. 3. Schematic locations of traps determined by DCTS and ICTS around the diced edge or the interface between the Si substrate and the passivation layer; (a) $V = 0$ V and (b) $V = V_R$.

$3.2 \times 10^{18}\,\mathrm{cm}^{-3}$.

From the $1/(T^2 t_{peak})$–$1/T$ plots, the values of E_t and σ_t for T_{DCTS} were determined to be $E_C - 0.54\,\mathrm{eV}$ and $1.4 \times 10^{-19}\,\mathrm{cm}^2$, respectively.

Since the reverse current was proportional to the square root of the reverse voltage, the generation current (I_g) was considered to be dominant. The effective lifetime (τ_g) was determined to be 2.7×10^{-5} s, since

$$I_g = \frac{qn_i WS}{2\tau_g}, \tag{5}$$

where n_i is the intrinsic concentration of Si and W is the steady-state depletion width.[5] On the other hand, τ_g can be approximately calculated using[5]

$$\tau_g \simeq \frac{1}{\sigma_t v_{th} N_t}, \tag{6}$$

because E_t is located around the midgap, where v_{th} is the thermal velocity. The values of τ_g for T_{ICTS} and T_{DCTS} are calculated to be 3.0×10^{-5} s and 1.1×10^{-7} s, respectively. Therefore, T_{ICTS} is considered to be a generation center.

Since the capture time (τ_t) is given by[6]

$$\tau_t = \frac{1}{n\sigma_t v_{th}}, \tag{7}$$

the value of τ_t for T_{DCTS} was calculated to be 0.30 s at room temperature, indicating that all T_{DCTS} can be refilled with electrons at 0 V for a period longer than 0.30 s. After the first DCTS measurement, it was kept at 0 V for 30 min and then the second DCTS measurement was performed. However, the transient reverse current was not observed, indicating that it was difficult to fill T_{DCTS} with electrons for 30 min at 0 V. This suggests that T_{DCTS} must be located in the region where n is much lower than $1.2 \times 10^{12}\,\mathrm{cm}^{-3}$ at 0 V.

T_{DCTS} is considered to be traps located in large-area defects, such as surfaces of the substrate, interfaces between the substrate and the passivation layer, micropiles, and grain boundaries in polycrystals. Since the Si substrate used here is a single crystal of good quality, T_{DCTS} is considered to be located at the surface of the diced edge or the interface between SiO_2 and the Si substrate.

The schematic locations of T_{DCTS} and T_{ICTS} are shown in Fig. 3. Both traps capture electrons at 0 V, while they emit electrons at V_R. However, it takes a long time for T_{DCTS} to capture electrons, when the applied voltage changes from V_R to 0 V.

In our Si pin diodes, N_t and E_t of large-area defects (i.e., traps at the surface of the diced edge or at the interface between the Si substrate and the passivation layer) were determined by DCTS, while those of point defects (i.e., generation centers) were determined by ICTS.

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