Jpn. J. Appl. Phys. Vol. 38 (1999) pp. L1015-L1017
Part 1, No. 9AB, September 1999

A New n-Channel Junction Field-Effect Transistor Embedded in the i Layer of a Pin Diode

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(Received June 9, 1999; accepted for publication July 12, 1999)

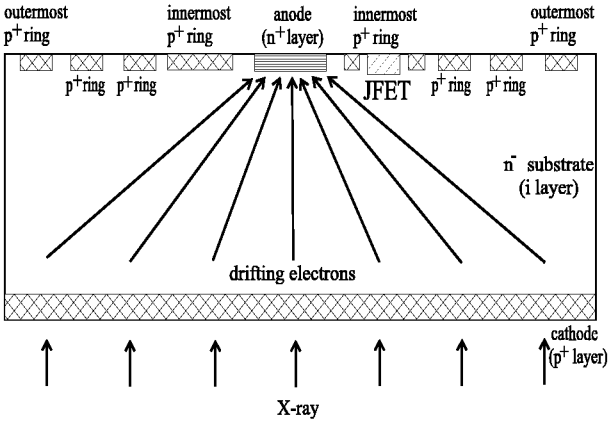
We experimentally confirmed a basic operation of the n-channel junction field-effect transistor (JFET) embedded in the i layer (n^- substrate) of a pin diode for X-ray detectors, which was proposed in Jpn. J. Appl. Phys. **37** (1998) L115. To electrically isolate the n-channel from the n^- substrate, a p^+ ring is formed around the JFET and is reverse-biased, instead of a deep p layer under the n-channel (i.e., the conventional structure). In the proposed structure, only one type of donor is ion-implanted in the n-channel, while in the conventional structure, both donor and acceptor are ion-implanted there. For the first time, the role of the p^+ ring in the electrical characteristics of the n-channel JFET is experimentally elucidated.

KEYWORDS: JFET, n-channel, new structure, front-end preamplifier for X-ray detectors, SDD, JFET embedded in pin diode

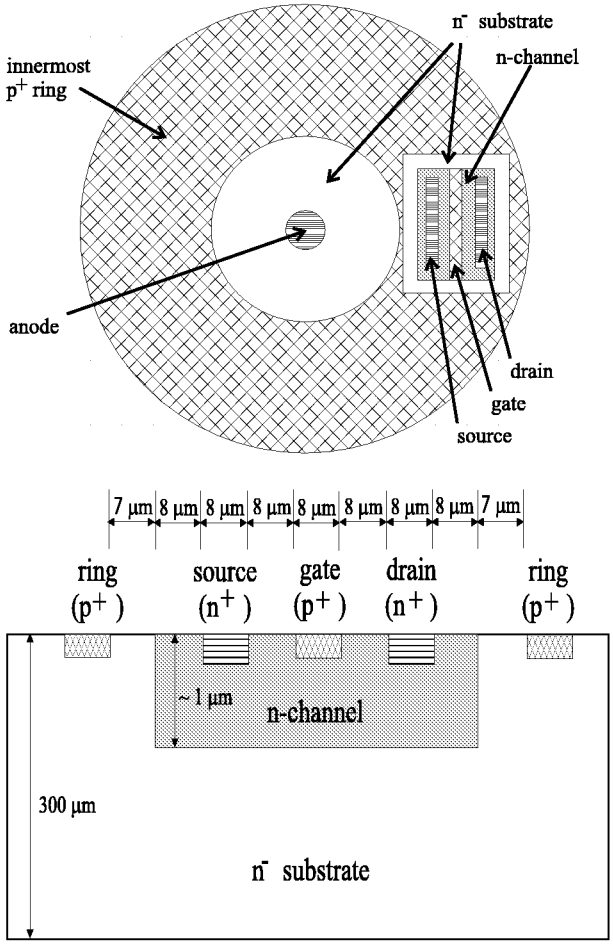
1. Introduction

Silicon drift detectors (SDDs) enable the realization of large-area X-ray detectors with spectroscopic energy resolution.[1,2] Since X-ray detectors are very sensitive to noise, we should avoid placing a long wire between a pin diode for an X-ray detector (X-ray pin diode) and a front-end junction field-effect transistor (JFET). For this reason, it is necessary to embed a JFET in the substrate (i layer) of the X-ray pin diode.

To take advantage of the electron mobility, which is much higher than the hole mobility, we should select an n-channel JFET as well as a high-resistivity n-type substrate (n^- substrate).



The schematic cross section of the proposed SDD is shown in Fig. 1, and the top view around the center is shown in Fig. 2. To reduce the capacitance of the X-ray pin diode, the area of the n^+ layer (anode)[3] is reduced. To form the depletion region over the whole n^- substrate, a high reverse-bias voltage (V_c) is applied to the p^+ layer (cathode)[3] of the X-ray pin diode. To effectively collect electrons produced by X-rays at the anode, several p^+ rings are formed at the surface and are reverse-biased. For example, -20 V and -100 V are applied to the innermost and outermost p^+ rings,



respectively, at $V_c = -100$ V.

To fabricate an n-channel JFET in the n^- substrate, a deep p region and a shallow n-channel region are usually formed.[4,5] This is because the deep p region isolates the n-channel from the n^- substrate electrically. In this conventional structure, however, ionized donors as well as ionized acceptors exist in the n-channel, suggesting that a lot of dopants generate noise[6] and reduce the

electron mobility in the n-channel at a low operating temperature.

Instead of the deep p region under the n-channel, we have proposed a new structure of an n-channel JFET with a p^+ ring around the JFET,[7] which is shown in Figs. 1-3. The proposed JFET is located in the innermost p^+ ring, as shown in Figs. 1 and 2. Because the donor density of the n^- substrate is rather low (about 2×10^{12} cm^{-3}), the depletion region formed by the reverse-biased p^+ ring spreads over the bottom of the n-channel. This is why it separates the n-channel from the n^- substrate electrically. As a result, the p^+ ring acts as a bottom gate of a four-terminal JFET which has a front gate and a bottom gate.

In this letter, we experimentally investigate the role of the reverse-biased p^+ ring in determining the electrical characteristics of the n-channel JFET.

2. Experimental

To form an n-channel in an n^- substrate of Si with a donor density of 2×10^{12} cm^{-3}, phosphorus (P) of 2×10^{10} cm^{-2} or 8×10^{10} cm^{-2} was ion-implanted with 500 keV. The peak position of the P distribution in Si was calculated to be about 0.8 μm from the surface, and the peak densities for the two types of doses were calculated to be about 5×10^{14} cm^{-3} and 2×10^{15} cm^{-3}, respectively.

Two 0.2-μm-thick n^+ layers (source and drain) were formed by the thermal diffusion of P. Then, two 0.15-μm-thick p^+ layers (gate and ring) were formed by the thermal diffusion of boron (B).

Each size of JFET is shown in Fig. 3. The gate length and width were 8 μm and 144 μm, respectively. The electrical measurement was carried out using three Keithley 236 Source Measure Units.

3. Results and Discussion

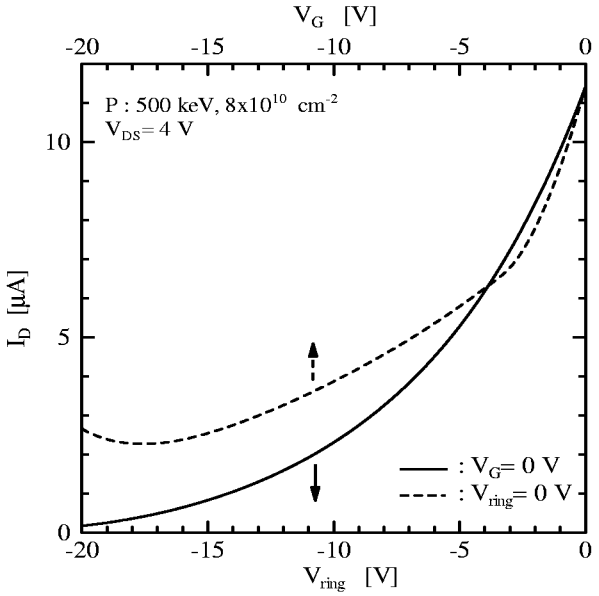


Figure 4 shows the influence of the p^+ ring voltage ($V_{\rm ring}$) as well as the gate voltage ($V_{\rm G}$) on the drain current ($I_{\rm D}$) at the drain-source voltage ($V_{\rm DS}$) of 4 V for the dose of 8×10^{10} cm^{-2}. In the figure, the solid and broken lines represent the $I_{\rm D} - V_{\rm ring}$ characteristics at $V_{\rm G} = 0$ V and the $I_{\rm D} - V_{\rm G}$ characteristics at $V_{\rm ring} = 0$ V, respectively.

First, we discuss the electrical isolation of the n-channel from the n^- substrate due to the reverse-biased p^+ ring. As is clear from the solid line, $V_{\rm ring}$ influenced $I_{\rm D}$, indicating that the p^+ ring affects the n-channel depth. As a result, the p^+ ring behaves exactly like a bottom gate of the four-terminal JFET, as proposed in our previous paper.[7] From the standpoint of the $I_{\rm D} - V_{\rm ring}$ characteristics, therefore, the n-channel is electrically isolated from the n^- substrate when the p^+ ring is reverse-biased.

The value of $I_{\rm D}$ decreased with $V_{\rm G}$ from -3 V to -17 V more slowly than it did with $V_{\rm ring}$. This suggests that at $V_{\rm ring} = 0$ V, the depletion region formed by the p^+ ring does not spread over the entire bottom area of the n-channel. Since the electronic built-in barrier between the n-channel and the n^- substrate is low, $I_{\rm D}$ consists of two types of currents through the n-channel as well as the n^- substrate just under the n-channel.

On the other hand, at $V_{\rm G} < -17$ V, $I_{\rm D}$ increased due to the reverse-bias current between the gate and the drain. This is because at $V_{\rm G} < -17$ V, the gate current ($I_{\rm G}$) flowed and $I_{\rm G}$ was the same as $I_{\rm D}$.

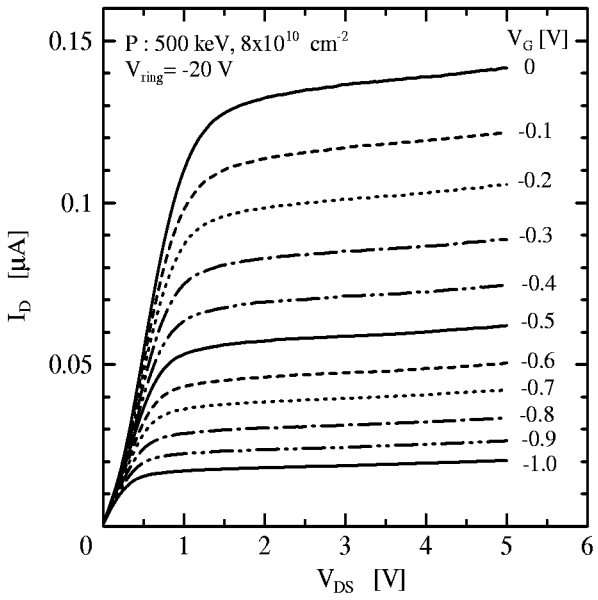
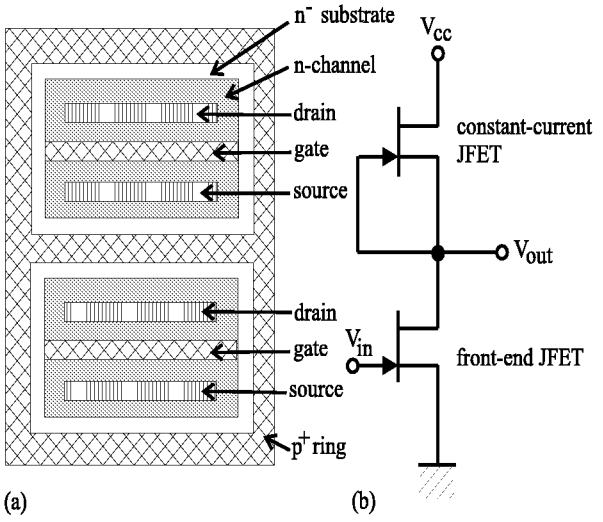


Figure 5 shows the $I_{\rm D} - V_{\rm DS}$ characteristics for 11 $V_{\rm G}$ at $V_{\rm ring} = -20$ V. According to the simulation, the depletion region in the n^- substrate spreads over about 100 μm at $V_{\rm ring} = -20$ V. As is clear from the figure, the typical $I_{\rm D} - V_{\rm DS}$ characteristics were obtained, and the saturation of $I_{\rm D}$ appeared clearly, indicating that the pinch-off occurred. Therefore, from the viewpoint of the $I_{\rm D} - V_{\rm DS}$ characteristics also, we have experimentally demonstrated that the reverse-biased p^+ ring can separate the n-channel from the n^- substrate electrically.

The electrical characteristics of the JFET for the dose of 2×10^{10} cm^{-2} were also measured. The pinch-off $V_{\rm ring}$ for the dose of 2×10^{10} cm^{-2} was about -7 V, while the pinch-off $V_{\rm ring}$ for the dose of 8×10^{10} cm^{-2} was less than -20 V.

Under the conditions of $V_{\rm DS} = 4$ V, $V_{\rm G} = 0$ V and $V_{\rm ring} = 0$ V, $I_{\rm D}$ was in the linear region, and the values of

I_D were 2.6 μA and 11.4 μA for the doses of 2×10^{10} cm^{-2} and 8×10^{10} cm^{-2}, respectively. The ratio of the latter I_D to the former I_D was 4.4. This ratio is reasonable because in the linear region, I_D is proportional to the donor density in the n-channel.[8)]



Since X-ray pin diodes are operated at a low temperature in order to avoid thermal noise, I_D should be low in order to avoid generation of heat. On the other hand, when I_D is low, it is difficult to obtain high transconductance ($g_m = \partial I_D/\partial V_G$). In order to obtain a high amplification factor, we propose the combination of the front-end JFET and a constant-current JFET in the innermost p$^+$ ring, as shown in Fig. 6, where the sizes of the two JFETs are the same. To obtain a constant current, the gate is connected to the source in the constant-current JFET. Since the input voltage (V_{in}) is around 0 V in the operating condition, the output voltage (V_{out}) is around half of the supplied voltage (V_{CC}). In the saturation region, the small ΔV_{in} can be converted into the large ΔV_{out}. For example, $\Delta V_{out}/\Delta V_{in}$ is estimated to be around 40 at $V_{CC} = 8$ V using the $I_D - V_{DS}$ curve at $V_G = 0$ V shown in Fig. 5. The lower the slope of I_D in the saturation region, the more $\Delta V_{out}/\Delta V_{in}$ is enhanced. According to the above discussion, the fabrication of the front-end JFET and the constant-current JFET are in progress. Moreover, in order to confirm the reduction of noise, SDDs with the two types of JFETs are being fabricated.

4. Conclusion

We investigated the role of the p$^+$ ring in the n-channel JFET proposed in our previous paper. In the JFET, instead of the deep p region under the n-channel, the p$^+$ ring is located around the n-channel. For the first time, we experimentally proved that the reverse-biased p$^+$ ring can separate the n-channel from the n$^-$ substrate electrically and that it acts as a bottom gate of the four-terminal JFET which has a front gate and a bottom gate.

Acknowledgements

We would like to express our gratitude to Mr. T. Utaka of Rigaku Industrial Corporation for his support during this work. This work is partially supported by Japan Science and Technology Corporation.

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Figure captions

Fig. 1. Schematic cross section of the X-ray pin diode with the proposed n-channel JFET.

Fig. 2. Schematic top view around the center with the proposed n-channel JFET.

Fig. 3. Schematic cross section of the proposed n-channel JFET in the n$^-$ substrate.

Fig. 4. Dependence of I_D on the reverse bias of the p$^+$ ring (solid line) or the gate (broken line) at $V_{DS} = 4$ V.

Fig. 5. $I_D - V_{DS}$ characteristics for 11 V_G at $V_{ring} = -20$ V.

Fig. 6. Front-end JFET and constant-current JFET: (a) schematic top view and (b) electrical circuit diagram.