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Fundamental Properties of MIS Solar Cells Using Mg-*p* Si System

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Existence of an inversion layer at the surface of Si in an MIS diode using Mg-*p* Si system is confirmed by the analysis of C^{-2}-V characteristics, and charges in the inversion layer are estimated. This diode is thought to behave like a p-n junction diode, since minority carrier current is dominant in I-V characteristics. Effects of oxidation time on the C^{-2}-V and I-V characteristics are studied. Photovoltaic properties of this inversion type MIS diode are measured.

§1. Introduction

Metal-insulator-semiconductor (MIS) structures have been studied[1-4] to improve the low open circuit voltage in metal-semiconductor (Schottky barrier) solar cells which had advantages such as low cost, low temperature fabrication and adaptability to semiconductor thin films. The MIS diode in which majority carrier current is dominant has larger dark saturation current (I_0) than the MIS diode in which minority carrier current is dominant. The latter MIS diode behaves like a p-n junction diode. If I_0 is smaller, the open circuit voltage (V_{oc}) becomes higher. In order to get higher efficiency, the latter MIS diode is expected to be fabricated. If the diffusion voltage is high and an inversion layer is formed at the surface of the semiconductor, the MIS diode can be thought of as a p-n junction diode with the above advantages. When silicon (Si) is used as a substrate semiconductor, a combination of magnesium (Mg) and *p* Si is a good one to fabricate the above diode, because the Mg-*p* Si system has high barrier height. In this report, we discuss fundamental properties of MIS solar cells using the Mg-*p* Si system and investigate the role of an insulator.

§2. Sample Preparation

Samples were prepared as follows. Wafers of *p* Si (100) with the resistivity of 6–12 ohm-cm were soaked in a solution of HF to remove SiO_2 and then rinsed in deionized water. As an ohmic contact for *p* Si, Au–Ga alloy was evaporated on the Si wafer and then alloyed at 400°C for one minute in the same vacuum system. Then, a very thin oxide film ($\simeq$10 Å) was prepared as an insulator by thermal oxidation in a dry oxygen flow at around 400°C. The Mg film was deposited on the oxide layer by vacuum evaporation in a vacuum of $2\text{–}4\times10^{-6}$ Torr. A silver-paste dot contact was attached to the Mg film. The sample size was 3.1 mm^2.

§3. Experimental Results and Discussion

3.1 *Capacitance-voltage characteristics*

Dark C^{-2}-V characteristics of the MIS diodes are shown in Fig. 1. These diodes have very thin oxide layers made at 400°C and Mg films of about 140 Å thick. In Fig. 1, the diffusion voltages (V_{D0}) obtained by extrapolation of the C^{-2}-V characteristics in the high reverse bias region are 0.91, 1.1 and 0.75 V for samples with oxidation time of 15, 30 and 45 min, respectively. But the diffusion voltages (V'_{D0}) obtained in the low reverse bias region (0 to -1.5 V) are 0.77, 0.87 and 0.60 V, respectively. The value of ψ(inv) defined by $(2kT/q)\ \ln\ (N_A/n_i)$[5] for the substrate with $N_A = 1.3\times10^{15}$ cm^{-3} is 0.59 V using $n_i = 1.5\times10^{10}$ cm^{-3}. Since V_{D0} is higher than ψ (inv), these diodes seem to have an inversion layer at the surface of Si.

The extrapolated values of C in the low reverse bias region using the C^{-2}-V characteristics in the high reverse bias region are smaller than the experimentally observed values. This is thought to be caused by the following effects: 1) effect of capacitance (C_i) of the very thin oxide film in series; 2) effect of diffusion capacitance (C_{diff}) in parallel; 3) effect of capacitance (C_{ss}) due to surface states in parallel; 4) effect due to the existence of the inversion layer. The capaci-

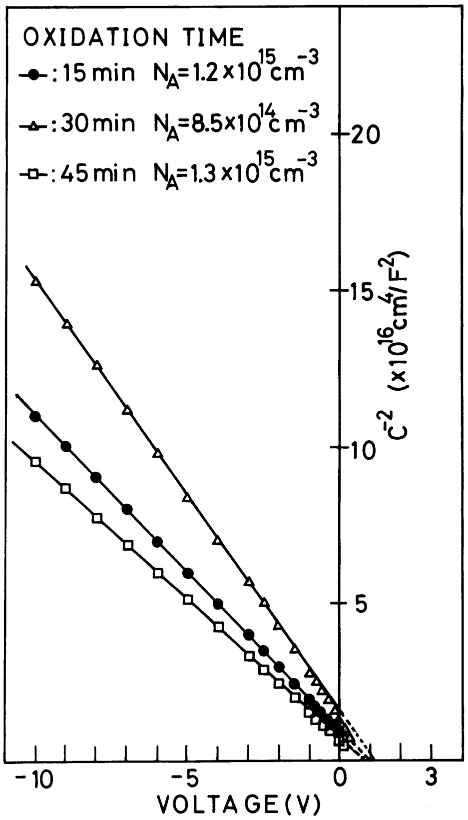

Fig. 1. Capacitance-voltage characteristics.

tance C_i or C_{diff} does not give the feature like the C^{-2}-V characteristics in Fig. 1. Contribution of the capacitance (C_i) is negligible, since the thickness of the oxide layer measured by ellipsometry is about 10 Å and the value of the capacitance is very large. Although C_{diff}, which is proportional to exp (qV/kT)[6], changes very rapidly with bias voltage (V) in the low reverse bias region, the difference between the capacitances obtained by extrapolation and measured experimentally does not change so rapidly with bias voltage. Effects of both 3) and 4) are discussed together, since it is difficult to distinguish them. The total charge Q in the semiconductor is given by $Q=Q_D+Q_R$. Here, Q_D, a function of voltage, is the charge of ionized acceptors in the region from the surface to the end of the depletion region, and Q_R is the sum of the charge Q_I stored in the inversion layer and the charge Q_{ss} in the surface states. Here, Q_{ss} changes with bias voltage, and Q_{ss} is put as zero at zero bias.* Electrons are thought to flow between metal and Si easily since the oxide layer is very thin, and it seems to be difficult for many electrons to be stored in the surface region of Si at high reverse bias. The electron quasi-Fermi level is assumed to be pinned with the metal Fermi level.[7] Therefore, the charge in the surface states for electrons does not change with bias voltage. Since the hole quasi-Fermi level seems to be near or in the conduction band at the surface and surface states exist only in the band gap, the charge of the surface states for holes does not change so much with reverse bias voltage. Based on these arguments, Q_R seems not to change so much with reverse bias voltage, but Q_D increases with reverse bias voltage. Therefore, at high reverse bias, the total charge Q is given by $Q(V_h)=Q_D(V_h)$, since $Q_D(V_h) \gg Q_R(V_h)$. Hence, capacitance $C(V_h)$ in the high reverse bias region is given by

$$C(V_h)=\sqrt{\frac{\varepsilon_0\varepsilon_s qN_A}{2(V_{D0}-V_h)}} = \frac{\varepsilon_0\varepsilon_s qN_A}{\sqrt{2\varepsilon_0\varepsilon_s qN_A(V_{D0}-V_h)}}, \quad (1)$$

where,

$$Q_D(V_h)=\sqrt{2\varepsilon_0\varepsilon_s qN_A(V_{D0}-V_h)}. \quad (2)$$

Here, ε_0 is free space permittivity, ε_s semiconductor dielectric costant, N_A acceptor impurity concerntration and q electron charge. At low reverse bias, $Q_D(V_1)=Q(V_1)-Q_R(V_1)$, because $Q_R(V_1)$ cannot be negligible. Here, the total charge $Q(V_1)$ is given by extrapolation of eq. (2) to low reverse bias. Therefore, capacitance $C(V_1)$ in the low reverse bias region is given by

$$C(V_1)=\frac{\varepsilon_0\varepsilon_s qN_A}{Q_D(V_1)} = \frac{\varepsilon_0\varepsilon_s qN_A}{\sqrt{2\varepsilon_0\varepsilon_s qN_A(V_{D0}-V_1)}-Q_R(V_1)}. \quad (3)$$

Hence, the capacitance in the low reverse bias region becomes larger than the extrapolated value from the C^{-2}-V characteristic in the high reverse bias region using eq. (1).

Using data in Fig. 1, Q_R-V relations based on eq. (3) are shown in Fig. 2. The value of Q_R

*Because, the effect due to the charge stored in the surface states at zero bias is included in the diffusion voltage V_{D0} obtained by extrapolation of the C^{-2}-V characteristic in the high reverse bias region.

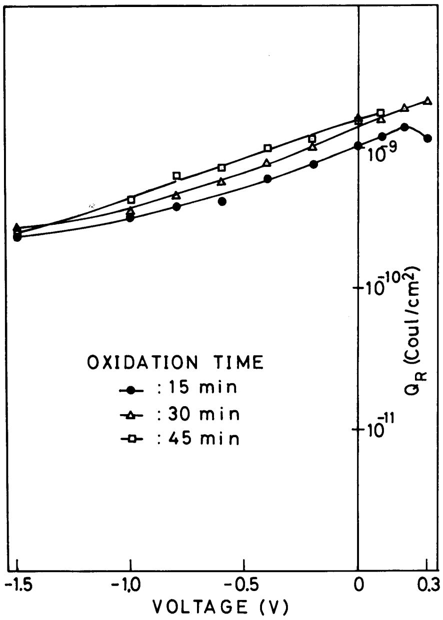

Fig. 2. Q_R-V relations.

increases slightly with bias voltage. At zero bias voltage, Q_R is equal to Q_I, since Q_{ss} is zero at zero bias voltage. Therefore, existence of the inversion layer at the surface of Si in the MIS diode using the Mg-*p* Si system is confirmed.

The diffusion voltage (V_{D0}) obtained by the C^{-2}-V method in the high reverse bias region varied with oxidation time. Since these diodes are made from the same Si wafer, all of the diffusion voltages (V_{D0}) must be the same. The main reason seems to be the difference in the surface state density. The surface state density is decreased with oxidation time shorter than 30 min, and is increased longer than 30 min.

3.2 *Current-voltage characteristics*

Dark log I-V characteristics shown in Fig. 3 change remarkably when oxidation time is changed. The ideality factor n defined by $n = (q/kT)\partial V/\partial \ln I$ varies with oxidation time. Current transport mechanism is analyzed in the inversion type MIS diode. There are four currents: majority carrier current I_{maj}; minority carrier current I_{min}; recombination current I_{rg} in the depletion region; and recombination current I_{rgs} at the surface of the semiconductor.[3] If the diffusion voltage is high and the inversion layer is formed at the surface of Si, I_{maj} is much smaller than I_{min} and I_{rgs} is negligible.[7] Therefore, the main currents are assumed to be I_{min} and I_{rg}. Minority carrier current I_{min} is given by

$$I = I_{min0}\left(\exp\left(\frac{qV}{kT}\right) - 1\right), \tag{4}$$

where,

$$I_{min0} = q\left(\frac{n_{p0}D_n}{L_n}\coth\frac{W_p}{L_n} + \frac{p_{n0}D_p}{L_p}\coth\frac{W_n}{L_p}\right). \tag{5}$$

Here, D_p and D_n are hole and electron diffusion constants, L_p and L_n hole and electron diffusion lengths, p_{n0} and n_{p0} the densities of free holes in the *n*-type region and of free electrons in the p-type region, and W_n and W_p the widths of the n- and p-type regions, respectively. The values of L_n and L_p are 200 μm and 90 μm given from the literature,[8] respectively, and the value of W_p is 300 μm from measurement of the wafer thickness. The value of W_n is the width of the inversion layer in Fig. 4 and given by

$$W_n = \sqrt{\frac{2\varepsilon_0\varepsilon_s V'_{D0}}{qN_A}} - \sqrt{\frac{2\varepsilon_0\varepsilon_s\psi(\mathrm{inv})}{qN_A}}. \tag{6}$$

The values of W_n obtained by the C^{-2}-V characteristics are 1.2×10^3, 1.8×10^3 and 64 Å for samples with oxidation time of 15, 30 and 45 min, respectively. Using the above values and approximate expression for hyperbolic cotangent, I_{min0} is rewritten as follows,

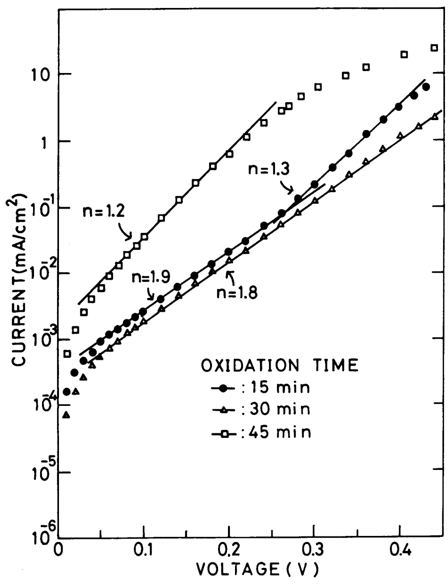

Fig. 3. Current-voltage characteristics.

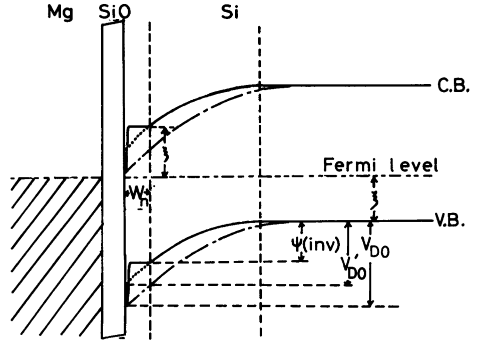

Fig. 4. MIS energy band structure. Solid line expresses the real energy band curve, dotted line expresses the energy band curve guessed from the low reverse bias region and dash-and-dot line expresses the energy band curve guessed from the high reverse bias region. The value of W_n is the distance between the surface and the position where the energy difference between the Fermi level and the conduction band is equal to the energy difference ξ between the Fermi level and the valence band at zero bias.

$$I_{\min 0}=q\left(\frac{n_{p0}D_n}{L_n}+\frac{p_{n0}D_p}{W_n}\right). \tag{7}$$

Using $D_n=30\ \text{cm}^2/\text{s}$, $D_p=10\ \text{cm}^2/\text{s}$[8] and n_{p0} given by n_i^2/N_A and by assuming that p_{n0} is equal to n_i^2/N_A,* the values of $I_{\min 0}$ are given as 25, 24 and 410 nA/cm^2, respectively. Experimentally observed values of I_0 are 41 nA/cm^2 for $n=1.3$ and 350 nA/cm^2 for $n=1.9$ for the diode with oxidation time of 15 min, 210 nA/cm^2 for the diode with oxidation time of 30 min and 1.7 μA/cm^2 for the diode with oxidation time of 45 min. From the above discussion and the value of the ideality factor, the main current in the diode with oxidation time of 15 min is diffusion current in the bias region for $n=1.3$, and recombination current in the bias region for $n=1.9$. The current in the diode with oxidation time of 45 min is also diffusion current. But, it is very difficult to determine whether diffusion or recombination current is dominant in the diode with oxidation time of 30 min. Because, the ideality factor implies recombination current, but the value of $I_{\min 0}$ implies diffusion current.

*The value of n_{n0} given by Q_R/qW_n are 5.2×10^{14}, 5.8×10^{14} and $1.5\times10^{16}\ \text{cm}^{-3}$ and they are nearly equal to the values of N_A. Since p_{n0} given by n_i^2/n_{n0} is nearly equal to p_{n0} defined by n_i^2/N_A, this is thought to be good assumption.

§4. Photovoltaic Properties

Photovoltaic properties of the MIS diode thought of as a p-n junction diode were investigated. Reflectances of thin Mg films on Si and transmittances of those on glass substrates were measured. The Mg film thickness was changed to get the large short circuit current, which gave the value of 140 Å for the optimum thickness.

Figure 5 shows relations between oxidation time and the open circuit voltage, the short circuit current and the fill factor illuminated by an incandescent lamp with $P_{in}=37\ \text{mW/cm}^2$. The good cell was fabricated with the efficiency of 3.2%, the open circuit voltage of 410 mV, the short circuit current of 4.7 mA/cm^2 and the fill factor of 60% for a substrate with the resistivity of 1–2 ohm-cm. Since the MIS solar cell using the Mg-*p* Si system has very high reflectance, large short circuit current cannot be obtained, and the cell needs an appropriate antireflective (AR) coating. Films of SiO with the thickness of 860 Å were deposited as an AR coating. The SiO film for Mg on Si is not so effective as the SiO film for Si, because the refractive index of SiO is 1.6. In calculation, the reflectance of Mg on Si can be decreased from 80% to 18% at the wavelength of 550 nm when a material with the refractive index of 2.6 is used as an AR coating. By simple calculation, the efficiency will be about 12%.

§5. Conclusion

In the MIS cell using the Mg-*p* Si system, existence of the inversion layer at the surface of

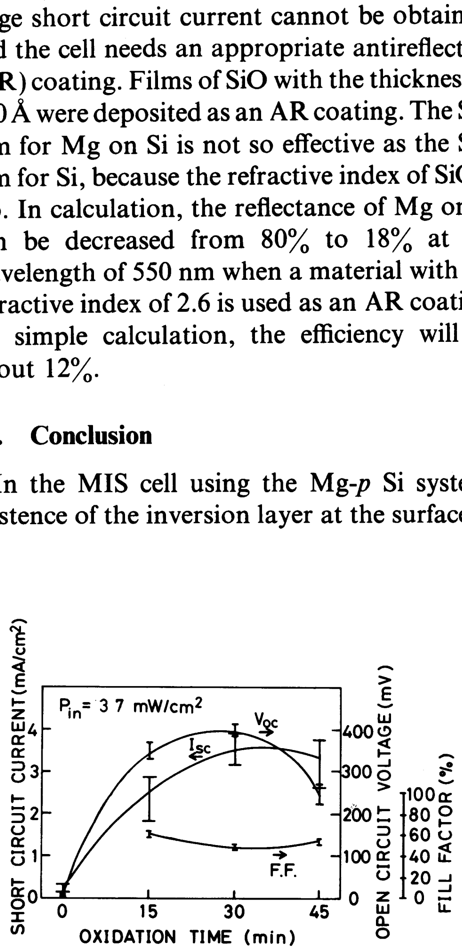

Fig. 5. Change of cell parameters for different oxidation time.

Si is confirmed by the analysis of C^{-2}-V characteristics. This diode is thought of as a p-n junction diode, since minority carrier current seems to be dominant in log I-V characteristics. Although photovoltaic properties are not very good without an AR coating, the Mg-*p* Si system has possibility of improvement in the short circuit current with an appropriate AR coating.

Acknowledgments

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